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Unique Bit-Error-Rate Measurement System for Satellite Communication Systems

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National Aeronautics
and Space Administration

**Scientific and Technical
Information Branch**

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Summary

Bit-error-rate measurements, necessary to assess the performance of communication systems and components, were required for the ground-based simulation and test bed of a Ka-band, satellite-switched time-division multiple access (SS-TDMA) satellite system at the NASA Lewis Research Center. This report discusses the requirements and design tradeoffs for that system and provides a description of its hardware design.

Introduction

Increasing demands for satellite communications will soon saturate the presently available frequency spectrum and the available geosynchronous orbital space. Consequently, in 1978 the NASA Lewis Research Center began an investigation of using the Ka-band (30-GHz uplink and 20-GHz downlink) for commercial satellite communications in the United States.

The program began with market and systems studies to determine the role of 30/20-GHz communication satellites. The studies determined that 30/20-GHz satellites would be necessary to relieve the orbital and frequency congestion as well as to maintain the United States' role as the world leader in satellite communications (ref. 1).

A technology development phase of 30/20-GHz hardware followed the market and systems studies. During this phase, several major components of the 30/20-satellite system were developed under technology contracts as proof-of-concept (POC) models (intermediate-frequency (IF) matrix switches, a baseband processor, receivers, antennas, and traveling-wave-tube-amplifier (TWTA) transmitters). Tests and evaluations of the POC models proved their functionality and demonstrated that developing 30/20-GHz communications satellite hardware was feasible.

Currently, NASA is developing a flight model and a laboratory model to demonstrate a complete 30/20-GHz satellite system. The flight model—the Advanced Communication Technology Satellite (ACTS)—is being developed in a cooperative effort with industry. This Ka-band satellite-switched time-division multiple access (SS-TDMA) satellite is scheduled for launch in 1990. The laboratory model—the system integration, test, and evaluation (SITE) project—is a ground-based simulation and test bed of a Ka-band SS-TDMA satellite system. The SITE system incorporates many of the POC models developed in the 30/20-GHz technology development phase.

SITE Project

The purpose of the SITE project is to construct a laboratory model of a satellite system to test and evaluate satellite and ground-segment components and subsystems and to exercise and evaluate networking algorithms. To realistically model a satellite system, most of the major functions and features of the system must either be designed or simulated. Within the SITE project, several major components of a TDMA communication satellite are being designed and constructed, including ground terminals and satellite transponders. Link simulation is being performed to investigate the effects of range delay and rain fade and to develop and test compensation techniques. Different networking schemes are being used to test network control and synchronization. The POC models will be integrated into the SITE project test bed for test and evaluation. All hardware and software necessary to integrate the POC components are being designed and constructed at Lewis. The SITE project, which will also provide a technical information base for the ACTS project, is described in greater detail in reference 2.

Bit-Error-Rate Measurements

A bit-error-rate (BER) measurement system is necessary to evaluate the performance of communication systems and components. This system can be used as an evaluation and debugging tool for digital components and subsystems, and it can provide a performance measure of radio frequency (RF) components and subsystems of digital communications systems. In addition, the BER measurement system can determine the effects that the total system—digital and RF components integrated together—has on transmitted data.

The BER is calculated from the total number of data bits transmitted through the device under test and the number of bits received in error:

$$\text{BER} = \frac{\text{Number of bits received in error}}{\text{Total number of bits received}}$$

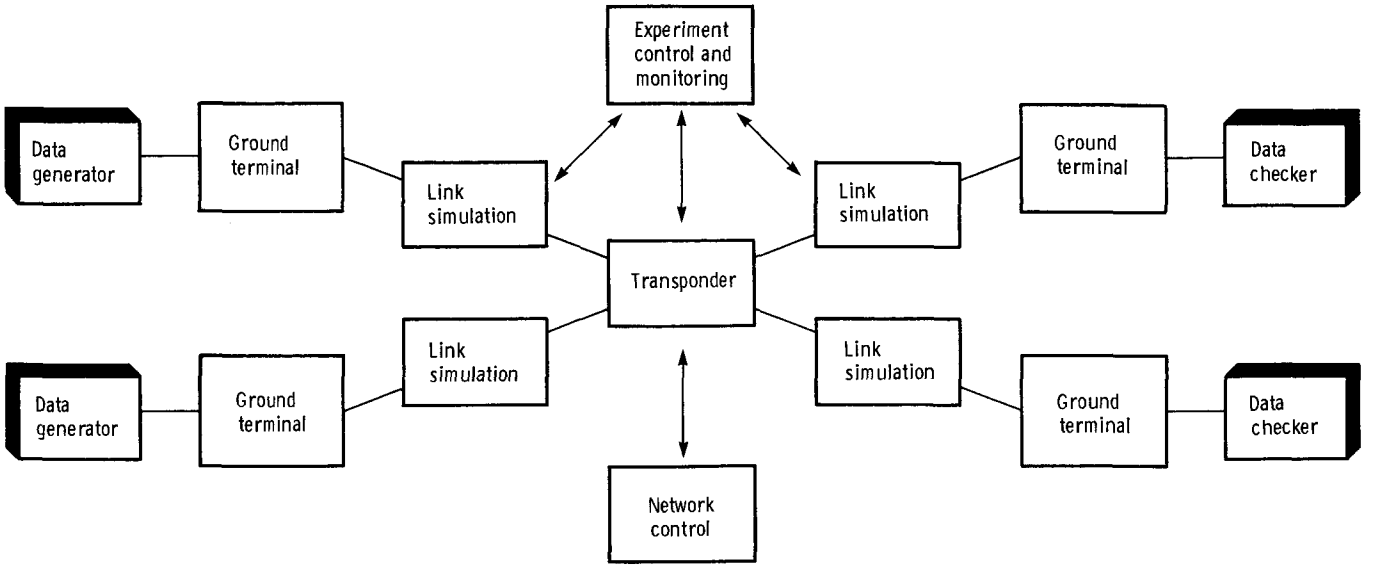

Figure 1.—SITE project block diagram.

A BER measurement system for the SITE project was needed to provide data source simulation and BER performance evaluation.

Figure 1 shows a block diagram of the SITE project system. The data generators and data checkers make up the BER measurement system. The data generators serve as the digital data sources for the system and the data checkers perform BER measurements on the received data.

Design Requirements

The data source for the BER measurement system is the data generator. It was required to create continuous pseudorandom serial data at one of several data rates ranging from 1 to 220 megabits per second (Mb/sec). The maximum data rate, 220 Mb/sec, was dictated by the POC modulators and demodulators selected for the SITE project. (The actual rate, 221.184 Mb/sec, is referred to as 220 Mb/sec for simplicity.) The data checker was required to compute BER's on the data created by the data generator. The expected BER range was 10^{-3} to 10^{-7}. The desired BER test durations were up to 1 hr of continuous operation.

The data generator and data checker were required to be controlled both manually and by a computer so that BER testing could be automated if desired. The data checker would relay the BER measurement data to the controlling computer so that the computer could compute the BER and then create graphs based on the BER. The controlling computer for the SITE project (the experiment, control, and monitor (EC&M) computer) provides control and data acquisition for several components and subsystems within the SITE project test bed, including power meters, variable RF attenuators, range delay simulator, signal generators, data generator, and data checker.

It was critical for the data generator and data checker to be operationally independent and low in cost. Independence would allow them to operate regardless of pairing, distance between units, and time delay between units. This independence was necessary because the data generator and checker could potentially be connected to two different ground terminals in two different locations. Low cost was a requirement because several data sources and BER measurement systems were required throughout the SITE project system.

Hardware Design

Three approaches for fulfilling the SITE project BER measurement requirements were investigated (fig. 2). The first approach, to purchase a commercial BER test set, could provide the required data rates and BER ranges. However,

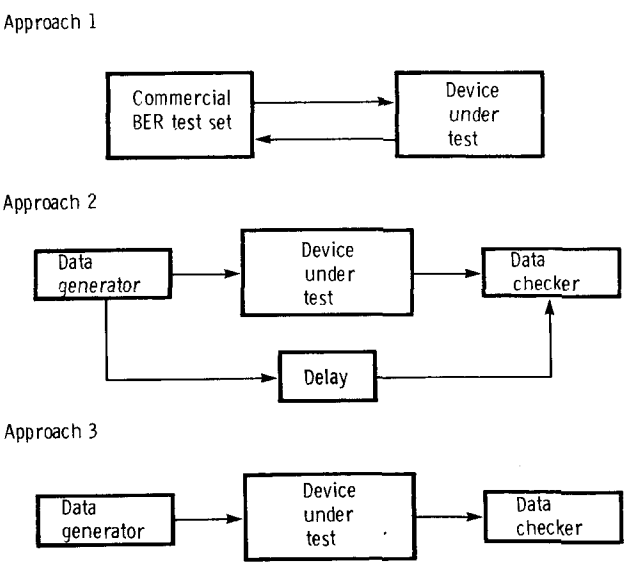

Figure 2.—Bit-error-rate test set options.

many commercial test sets could not provide source and receiver independence because they required the sending and receiving units to be in the same chassis. In addition, most of the available test sets were very expensive. The high cost would have precluded the use of multiple BER test sets.

The second approach, to design in-house a simple BER test set, would allow direct comparison between transmitted and received data. The transmitter portion of this kind of test set would require two separate ports, one to transmit data over the channel being tested and one to transmit data directly to the receiver. The extra port needs a variable delay associated with it so that received data could be synchronized to the directly transmitted data. The variable delay would have been difficult to implement for the wide range of test configurations planned in the SITE project and may have introduced additional bit errors.

The third approach, to design a BER test set with a data source that could create data with a reproducible pattern that could be derived from the data itself at the data checker, would require a more complicated design than the second approach but would allow the source and destination to be independent. This approach would be less expensive than buying a commercial BER test set. Consequently, this was the approach chosen for implementation.

Because the source and destination are completely independent, the data checker must know the content of the data created by the data generator for a comparison to be made. The data checker must be able to re-create the error-free contents of the transmitted data stream from the received data. To accomplish this, an error encoded control word is sent periodically within the transmitted data stream. From the control word, the data checker can derive enough information about the transmitted data stream to re-create the exact data pattern. The re-created data can then be compared to the received data to check for errors. Because the control word is transmitted within the data stream, the data generator and data checker do not need to be directly connected to each other. They can be operated independently so that any data checker can receive data from any data generator and so that the distance or time delay between the data generator and the data checker does not affect the operation.

To make implementation easier and to reduce cost, transistor-transistor logic (TTL) was used as much as possible in the data generator and data checker designs; thus, faster clock rates and harder to use emitter-coupled logic (ECL) were avoided. Special 64-bit parallel-to-serial (P/S) and serial-to-parallel (S/P) converters were used in the data generator and data checker, respectively, to reduce the use of ECL. The converters are the only portions of the two designs that operate at the full serial data rate. These single board, 64-bit converters allow the data rate of the other data generator and data checker hardware to be much slower, at TTL speeds. The P/S and S/P converters were designed at Lewis using a combination of ECL (10K and MECL III) and TTL. This design permitted the interface between the data generator and data checker and the P/S and S/P converters to be at TTL levels.

Data Generator

Pseudorandom data are produced in the data generator from the outputs of two 8-bit counters. One 8-bit data-creation counter counts up and the other counts down. The counters are clocked once every word (each word being 64 bits long). Every 256 words, the down counter is given one up-count clock pulse to shift the relationship between the outputs of the up counter and the down counter. The data-creation method produces a data stream that repeats every 65 536 words.

Data words are created from the data-creation counters by mapping the 16-bit counter outputs into a 64-bit word (fig. 3). The mapping is performed by hardwiring each of the 16 counter outputs to a few of the bits in the 64-bit words.

The initial contents of the two counters can either be fixed or random. The starting counts can be loaded either from two 8-bit dip switches or from the outputs of four 4-bit counters that are clocked asynchronously with respect to the rest of the data-generator timing. The initial count on the four 4-bit counters is random, the value that the outputs assume when the power is turned on. The data-creation counters are loaded when the reset pulse is given to the data generator.

The data generator creates a control word that enables the data checker to reproduce the transmitted data stream. The control word is created from the initial count (when the data generator is started) on the two 8-bit data-creation counters. The 16-bit counter outputs are error encoded using a modified Hamming code (fig. 4). The 16 bits are divided into six units, five containing 3 bits and one containing 1 bit. Two bits are added to the last unit, one is a stop flag (to be discussed later) and the other is a 0, making it a 3-bit unit. Each unit is encoded with four parity check bits. The Hamming encoding method allows the data checker to detect 2-bit errors and correct 1-bit errors in each of the six units.

The control word is the first word sent in the data stream, and it is sent periodically within the pseudorandom data stream thereafter. Dip switches can select the number of 64-bit data words *DW* between control words *CTW*—65 536 words or less.

$$CTW\ DW_1\ DW_2 \ldots DW_n\ CTW\ DW_{n+1} \ldots$$
$$|\leftarrow 2 \text{ to } 65\,536 \text{ words} \rightarrow|$$

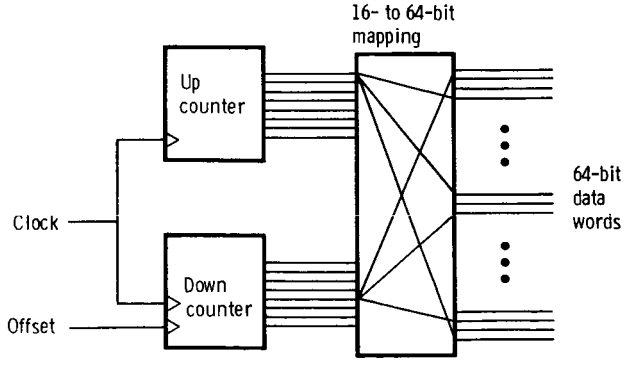

Figure 3.—Data-creation counters and mapping.

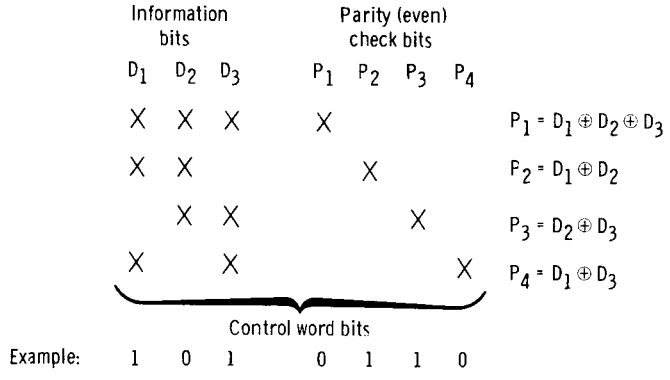

Figure 4.—Control word error-encoding method.

A multiplexer is used to select between data and control words. The number of data words between control words must be the same for the data generator and data checker so that fictitious errors are not counted.

The control word has one additional function. A stop flag can be sent within the control word to signal the data checker that the data generator has stopped sending data. When the data generator gets a stop pulse either manually or from the controlling computer, it sets the stop flag in the next control word and stops sending data one data word before the next control word. The data checker checks the stop flag in every control word. If the stop flag is set, the data checker stops one data word before the next control word. Thus, the data generator and checker stop at the same point in the data stream, and the data checker does not calculate BER's on invalid data.

The format of the control word is illustrated in figure 5.

A serial data stream is created by transferring the 64-bit parallel data words and control words to the P/S converter. The converter shifts the 64-bit parallel data into a serial stream at data rates up to 220 Mb/sec.

The heart of the data generator timing and control is a single 4-bit binary counter. The counter clock rate is one-fourth the serial data rate. Since the highest data rate required of the data generator is 220 Mb/sec, the fastest clock rate for the binary counter is 55 MHz. Combinational logic is used on the counter outputs to create the desired signals to control the rest of the data generator hardware. A block diagram of the data generator is shown in figure 6.

Data Checker

The data checker receives serial data through the S/P converter. The serial data is converted into 64-bit parallel data words by the S/P converter.

As stated previously, to count the number of bits in error, the data checker must be able to regenerate the exact data pattern that the data generator transmits. The received and regenerated data words can then be compared to each other, bit by bit, to get a count of the number of bits in error. The data checker gets the information about the transmitted data stream from the control word within the data stream. The data checker knows that the control word is the first word it receives and it knows the periodicity of the control word multiplexed

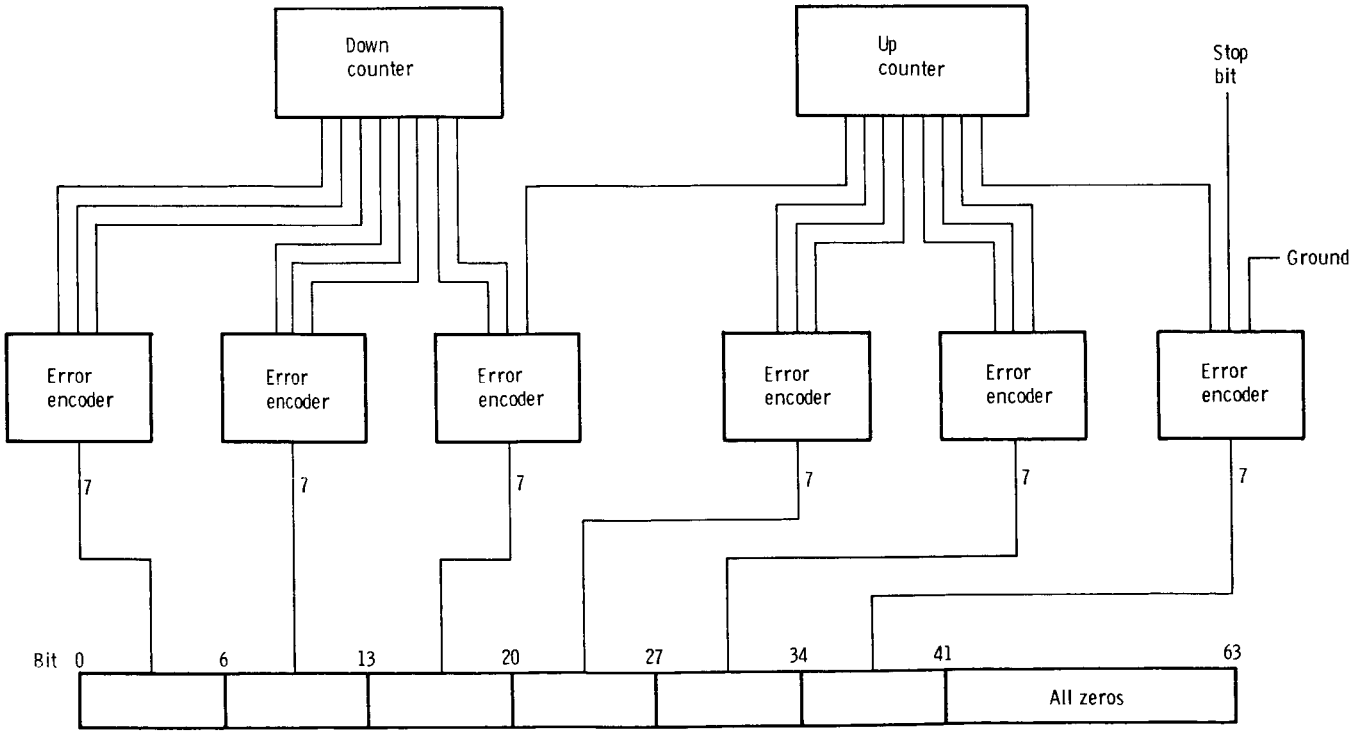

Figure 5.—Control word format.

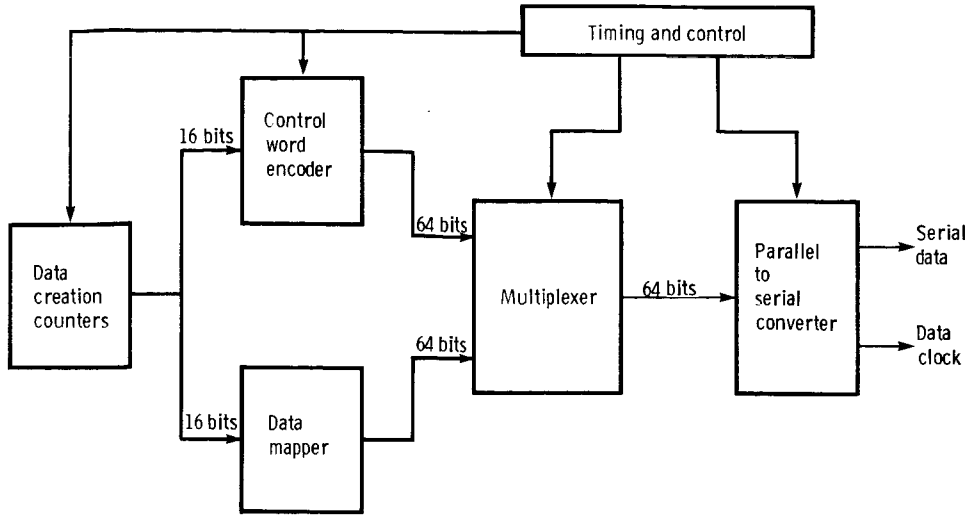

Figure 6.—Data-generator block diagram.

within the data. The distance between control words is set on dip switches to agree with the settings of the corresponding data generator switches.

When a control word is received, the data checker passes it to the error detection/correction circuit. The error detector divides the control word into the six groups. Syndrome bits are created from the parity of special groupings of the bits in each group. These syndrome bits identify if there is a single bit error, a multiple bit error, or no bit errors. If a single bit error is detected, the error detector identifies which bit is in error and it is flipped to the correct state by the error correction circuit. If a double error is detected, the Hamming code is not able to identify which bits are incorrect. If the control word contains any such noncorrectable bit errors, the control word is ignored and the data checker waits for the next control word. An even number of errors occurring in the control word groups are treated the same as a double error. Any odd number of errors greater than one are incorrectly detected as one error, and therefore are erroneously corrected. However, for even three errors to occur, the BER would have to be greater than 4×10^{-1}. Once a correct or correctable control word is received, BER checking begins. The error detection method is described in figure 7.

When a valid or correctable control word is received, the information portion of the control word is loaded into two 8-bit counters. The 8-bit counters are identical to the data creation counters in the data generator. The outputs of these counters are mapped into 64-bit words creating a regenerated version of the data that the data generator transmitted. After the counters are loaded, they create data, and all bits in subsequent control words are ignored except for the stop flag.

The data checker uses exclusive-OR gates to compare (64 bits at a time) the data it receives to the data that it regenerates. The result of the comparison is a 64-bit word in which every 1 indicates that a bit is received in error. The number of 1's need to be added to determine the total number of bit errors in that word.

The number of errors in each word are counted by breaking the 64-bit output of the comparator circuit into eight 8-bit groups. The 8 bits of each of the eight groups are loaded into 8-bit shift registers. The shift registers are clocked at one-eighth the data rate. The serial output of the shift registers is ANDed with the inverse of the shift clock and becomes a clock input to a binary-coded decimal (BCD) counter. Each clock pulse corresponds to a bit in error. Each of the 8-bit counters then contains a count of the number of errors in the corresponding 8-bit group of comparator outputs.

The outputs of the eight counters are added together using full adders to obtain a sum of the number of errors in each word. A running total of the number of bit errors is found by adding the number of errors for each word to the previous total number of bit errors. Bit errors detected in the control words become carry-in inputs to the full adders and are added to the number of errors in the word immediately following

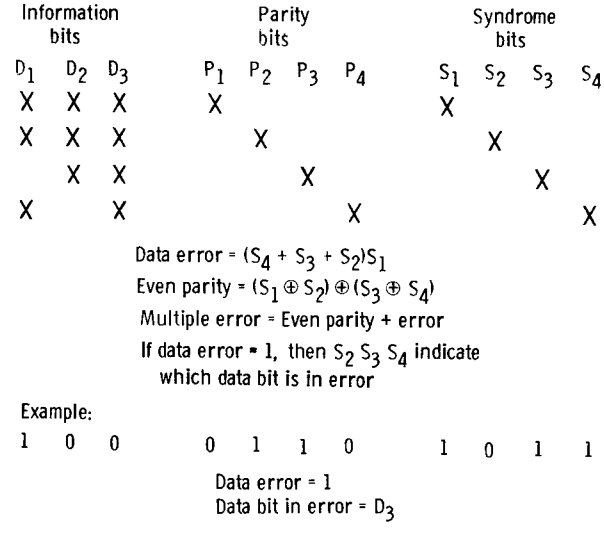

Figure 7.—Error detection/correction method.

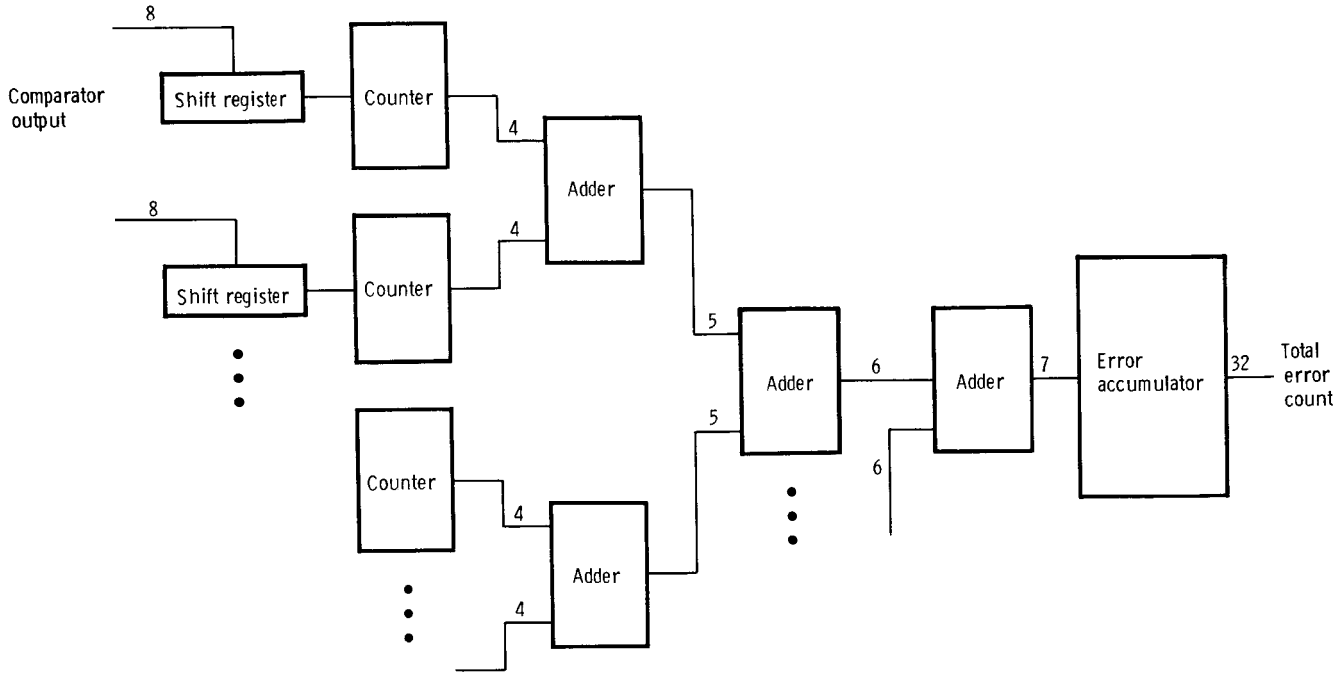

Figure 8.—Error-counting circuit.

the control word. A block diagram of the error-counting circuit is shown in figure 8.

To compute the BER, one must count the number of total bits received in addition to the number of bits in error. Instead of counting the total number of received bits, the data checker counts the number of received words. This allows a smaller TTL counter to be used. The size of the word counter and the size of the error-counting circuit were determined to meet the BER range and test duration requirements.

The BER can be calculated by two different methods. For one method, a hardware calculation is performed and the resulting BER is displayed on the data generator/data checker front panel. This method is discussed in the section **Display**. For the other method, the controlling computer performs a software calculation. In this case the number of bits in error and the number of words received are transferred to the controlling computer.

Just as in the data generator, the heart of the data checker timing and control circuit is a single 4-bit binary counter. The clock rate of the counter is one-fourth the data rate, making the maximum clock rate 55 MHz for 220 Mb/sec data. Combinational logic is used on the outputs of the counter to create all the necessary timing and control signals. A block diagram of the data checker hardware is shown in figure 9.

Display

A hardware BER calculation is performed for the display on the front panel of the data generator/data checker chassis. The hardware circuit uses the bit error count and a 100-bit count to calculate the BER.

The display consists of two parts, the mantissa and the exponent; the BER is displayed in scientific notation. The mantissa portion always displays the three most significant nonzero digits of the bit error count. A three-digit window is moved every time the next most significant digit becomes nonzero. The exponent portion is formed from a count of the total number of bits received. The exponent is also modified each time the mantissa window is shifted.

A numerical example of the BER calculation is

$$\text{Number of bits in error} = 824\ 567$$

$$\text{Number of bits received} = 10\ 00\ 000\ 000$$

$$\text{BER} = \frac{824\ 567}{10\ 000\ 000\ 000} = 8.34567 \times 10^{-5}$$

A block diagram of this calculation is shown in figure 10.

Clock Board

The desired multiple data rates are provided by a clock board containing several oscillators at different frequencies and several clock divider circuits. The clock board provides several fixed rates as well as a variable-rate clock source. Table I lists the available data rates and figure 11 shows a block diagram of the clock board.

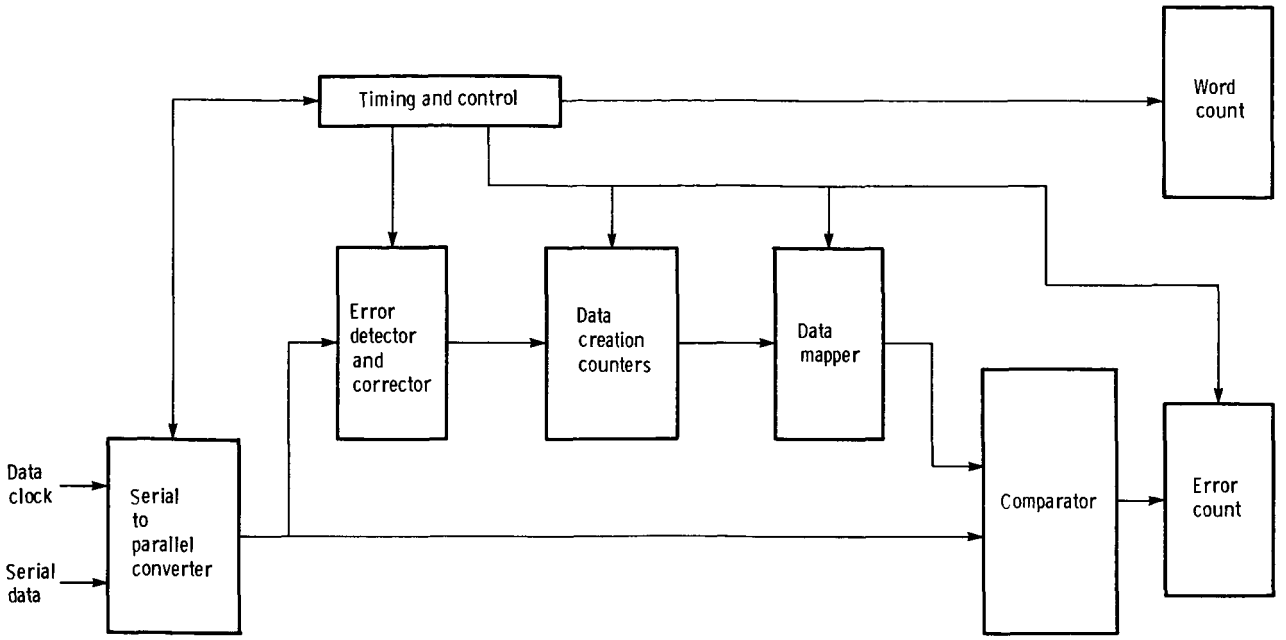

Figure 9.—Data-checker block diagram.

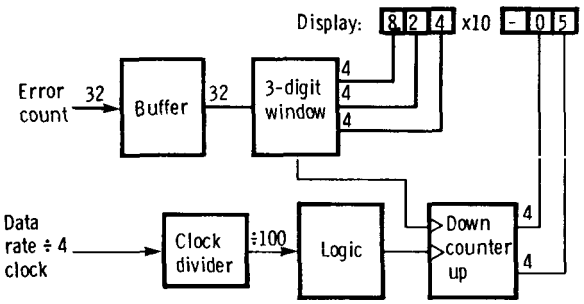

Figure 10.—Display board block diagram.

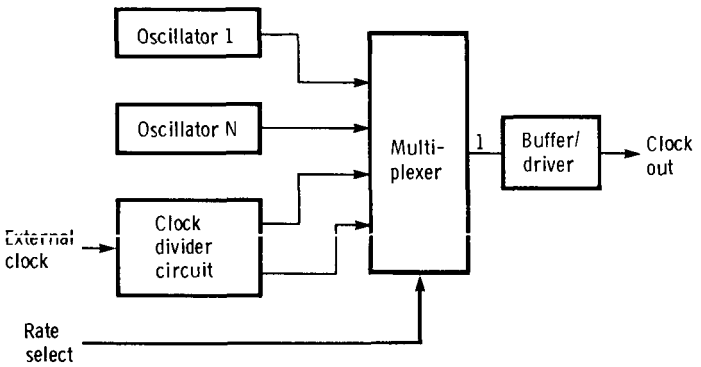

Figure 11.—Clock board block diagram.

TABLE I.—CLOCK BOARD RATES

Clock board rate, MHz	Description
1.25	General purpose
1.544	Telecommunications rate T1
5.00	General purpose
6.132	Telecommunications rate T2
12.5	General purpose
16.1079	Digital video
25.0	General purpose
42.95	Digital video
44.736	Telecommunications rate T3
50.0	General purpose
100.0	General purpose
200.0 (or variable)	General purpose

Operation

The data generator and data checker can be controlled either manually or by a computer. In either case, the necessary control signals are identical. Both the generator and the checker need to be initialized with a low-going RESET pulse. After initialization, data flow is started with a low-going SEND pulse given to the data generator.

The outputs of the data generator are the serial data stream, a corresponding data clock, and a control signal called the VALID DATA PULSE (a one-time pulse that signals the start of valid data). The data checker requires these three input signals to work properly. Data checking begins when it receives a VALID DATA PULSE. The BER calculation can be terminated by giving a low-going STOP pulse to the data generator causing the data generator to set the stop flag within the control word. Computer or manual control can be selected with a toggle switch on the data generator/checker front panel. The hardware BER calculation is displayed on the front panel whether the hardware is under computer control or not.

Hardware

The data generator and data checker were constructed on high-speed wirewrap circuit boards. The data generator design was built on one wirewrap board, the data checker design on two wirewrap boards. The clock board was constructed on a combination wirewrap/printed circuit board. The printed circuit portion, necessary because of the high-rate oscillators present in the design, was constructed on a simple two-sided board and mounted in a piggyback fashion on the wirewrap portion of the clock board design. The P/S and S/P converters are separate circuit boards. The present version was constructed using the Multiwire[1] process. The S/P and P/S designs were found to be somewhat unreliable and therefore are being replaced by a new design constructed on a special high speed wirewrap board using 100K series ECL logic. All the data generator/data checker boards were mounted in a 5-slot chassis (fig. 12).

Performance

BER's ranging from 10^{-12} to 10^{-2} can be calculated with the data checker. If the BER is less than 5×10^{-5}, tests using the data generator and the data checker can be run continuously for 3.5 days before the data checker word counters overflow. If the BER is greater than 5×10^{-5}, the error counter will overflow before 3.5 days. Table II shows the BER and corresponding length of time before the error counter will overflow.

To date, twelve data generators and data checkers have been constructed and tested. Half of these are presently in use for various applications. One set has been installed in a simple continuous-data SITE project ground terminal with modulation and demodulation. This ground terminal has been successfully used for traveling-wave-tube testing (ref. 3) and satellite transponder testing. Other data generator and checker sets have been very useful in debugging and testing digital hardware such as the SITE project TDMA ground terminals and the range delay simulator. The data generator and the data checker operate reliably even in electromagnetically and thermally hostile environments.

TABLE II.—ERROR COUNTER OVERFLOW

Bit error rate	Count duration
1×10^{-2}	32 min
1×10^{-3}	5.9 hr
1×10^{-4}	2.26 d
1×10^{-5}	22.6 d

Concluding Remarks

The system integration, test, and evaluation (SITE) project of the NASA Lewis Research Center required a flexible, low-cost method to perform multiple bit-error-rate (BER) calculations for system and component performance evaluation. The unique testing requirements precluded the use of commercially available BER test sets. Therefore, a special BER test set called the data generator and data checker was designed at Lewis.

The data generator and data checker are capable of producing data and performing error checking on pseudorandom serial data at rates up to 220 Mb/sec. The data

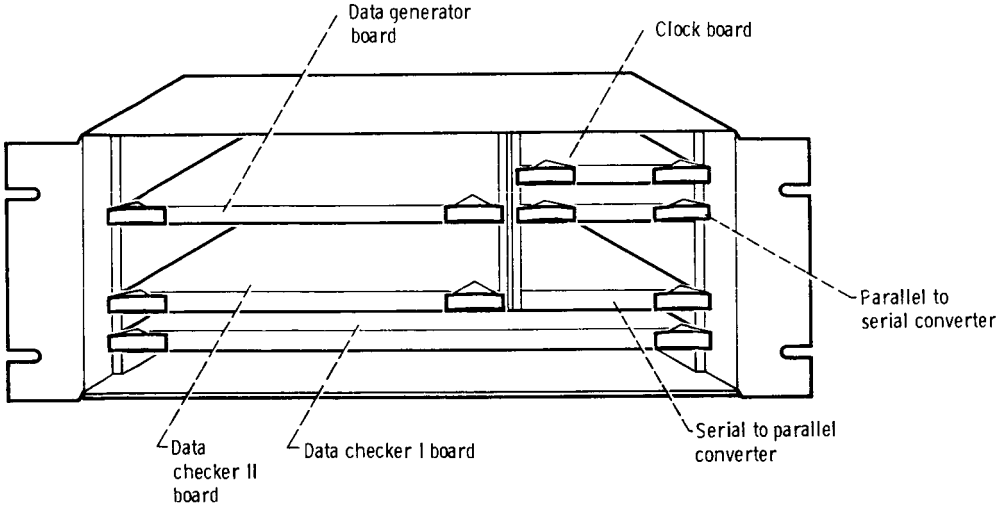

Figure 12.—Data generator/checker chassis layout.

[1]Multiwire is a tradename of the Kollmorgen Corporation.

generator and data checker are unique because the transmitter and the receiver need not be co-located. They can work regardless of pairing, distance between them, and time delay between them. BER's from 10^{-12} to 10^{-2} can be calculated with the data checker. Tests can be run up to 3.5 days at a BER of 5×10^{-5} or less.

The data generator and data checker have been installed in a continuous-data ground terminal with modulation and demodulation which has been successfully used for traveling-wave-tube and satellite transponder testing. Other data generator and checker sets have been used to debug and evaluate SITE project digital hardware.

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Lewis Research Center
Cleveland, Ohio, December 19, 1986

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15. Supplementary Notes

16. Abstract

Bit-error-rate measurements, necessary to assess the performance of communication systems and components, were required for the ground-based simulation and test bed of a Ka-band, satellite-switched time-division multiple access (SS-TDMA) satellite system at the NASA Lewis Research Center. This report discusses the requirements and design tradeoffs for that system and provides a description of its hardware design.

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